i281CPU

Senior Design — Team 14

Periodic Report 04

Reporting Period: October 9th through October 22nd

Team Members:

- Daryl Damman - Team Lead
- Logan Lee - Testing & Prototyping
- Grant Nordling - Parts Management & Quality Control
- Braxton Rokos - PCB Routing & Prototyping
- Gavin Tersteeg - Quality Control & Testing

Progress Summary

In our first meeting with our client, Dr. Stoytchev, we spent a large portion of our meeting discussing electronic parts that we still need to meet our goals. This included LEDs, chips, wires, switches, and chip erasers. We discussed the creation of a technical binder that would our schematics, designs, and relevant documents. We considered multiple design specifications for bus splitting. We agreed to use filter caps to reduce noise in our design. We further discussed control table visualizations. Methods for implementing the clock were discussed. The main issue raised was switching the clock speed. After this meeting, we built 4 MUXs and diagrams for our standards in breadboard wiring and LED light designation.

In the second meeting of this period with Stoytchev, we discussed more parts to order, diagrams to make, test protocol, tasks for the week, register implementations, EEPROM, DMEM, boot sequence, and schematics to make. The team will write more diagrams for design standards to increase work efficiency. For test protocol, we discussed making a test standard to reduce risk of damaging boards. We were tasked with starting work on more MUXs, the program counter, and designing the DMEM, EEPROM, and schematic for the PC update logic register implementation. We talked about module location and processor functionality. The final topic for this meeting was affirming a boot sequence Daryl had come up with Dr. Stoytchev was acceptable.

Pending Concerns and Issues

Some designs we still need to go over are the clock, DMEM, and Video card. Each of these will require the team members responsible for them to create a few ideas of how to go about designing them. Then we need to go over them with the client to ensure they meet their goals and requirements.

We also need to start creating the design on the breadboards to not fall behind on our schedule. We also need to create them on KiCad so we can visually see the pin-to-pin connections easier.

Upcoming Plans for Next Period

For the upcoming period, we plan on creating the schematics and designs for most of the components of the CPU. We have most of the parts we will need to build it other than parts for the clock. We also plan on going over the design for the clock.

A partial implementation of the program counter and register file should be made before Thanksgiving break.

Accomplishments

Multiple MUXs have been developed and implemented, leading to the first round of testing. Testing was a success and all implemented MUXs operate as expected.

The Boot Sequence draft was finally approved by Dr. Stoytchev leading to the next round of technical discussions that must be discussed.

Individual Contributions

Daryl Damman

Developed the second and fourth MUX for the processor.
Wrote most of the Project Plan and Engineering Design document.
Coordinated the Boot Sequence development.
Wrote templates for reports, user guides, and binder components.

Logan Lee

Began theoretical work on clock circuit design.
Developed the initial Gantt chart for the Project Plan Document.

Grant Nordling

Aided with documentation efforts and finalized the Project Plan and Engineering Design document.

Braxton Rokos

Aided with documentation efforts and wrote a large portion of the Project Plan presentation.
Completed the third and fifth MUXs for the processor.
Wrote the summary of Weekly Report 3.

Gavin Tersteeg

Lead technical discussions with the client.
Provided the required commentary for both Engineering Design and Project Plan presentations.
Developed the CMEM module and coordinated the Boot Sequence development.